AMENDMENTS TO THE SPECIFICATION

Please replace the Title with the following Title:

MICROPROCESSOR THAT DETECTS ERRONEOUS SPECULATIVE PREDICTION OF BRANCH INSTRUCTION OPCODE BYTE

Please delete the section entitled "SUMMARY" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

The present invention provides a branch prediction method and apparatus that makes efficient use of chip real estate, but also provides accurate branching early in the pipeline to reduce branch penalty. Accordingly, in attainment of the aforementioned object, it is a feature of the present invention to provide a microprocessor. The microprocessor includes a branch target address cache (BTAC), configured to cache, for each of a plurality of previously executed branch instructions: a prediction of whether the branch instruction will be taken and is present in a cache line of instruction bytes provided by an instruction cache in response to a fetch address, a target address of the branch instruction, and a location of an opcode byte of the branch instruction within the cache line. The BTAC is further configured to provide the prediction, the target address, and the location in response to the fetch address. The microprocessor also includes an instruction buffer, coupled to receive the cache line from the instruction cache and to mark a byte in the cache line within the instruction buffer indicated by the location provided by the BTAC if the microprocessor branches to the target address provided by the BTAC based on the prediction. The microprocessor also includes an instruction decoder, coupled to the instruction buffer, configured to format the instruction bytes in the cache line into formatted instructions. The microprocessor also includes prediction check logic, coupled to the instruction decoder, configured to indicate the microprocessor erroneously branched to the target address if the instruction decoder indicates the marked byte is in a non-opcode location within one of the formatted instructions.

In another aspect, it is a feature of the present invention to provide a method for correcting a branch instruction misprediction in a microprocessor. The method includes caching in a branch target address cache (BTAC), for each of a plurality of previously executed branch instructions: a prediction of whether the branch instruction will be taken and is present in a cache line of instruction bytes provided by an instruction cache in response to a fetch address, a target address of the branch instruction, and a location of an opcode byte of the branch instruction within the cache line. The method also includes the instruction cache providing the cache line to an instruction buffer in response to the fetch address. The method also includes the BTAC providing the prediction, the target address, and the location in response to the fetch address. The method also includes branching to the target address provided by the BTAC based on the prediction. The method also includes marking a byte in the cache line within the instruction buffer indicated by the location provided by the BTAC. The method also includes an instruction decoder formatting the instruction bytes in the cache line into formatted instructions. The method also includes indicating the microprocessor erroneously branched to the target address, if the instruction decoder indicates the marked byte is in a non-opcode location within one of the formatted instructions.

An advantage of the present invention is that it ensures proper program execution in a processor that employs a speculative BTAC, which has the potential advantages of more efficient use of integrated circuit real estate, improved processor cycle time and/or reduced processor clocks per instruction, and improved likelihood of single-cycle BTAC cache realization.